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Guideline for Gate Oxide Reliability and Robustness Evaluation Procedures for Silicon Carbide Power MOSFETs

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GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION PROCEDURES FOR SILICON CARBIDE POWER MOSFETS

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Foreword

This document was drafted by the JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use by SiC product suppliers and related power electronic industries. It provides guidelines for evaluating gate reliability and lifetime testing for silicon carbide (SiC) based power devices with a gate oxide or gate dielectric. The information is for manufacturers of SiC power devices, for quality evaluation and lifetime prediction purposes.

Introduction

This document has the purpose of laying out generally acceptable practices for testing gate oxide reliability of silicon carbide (SiC) based power devices having a gate dielectric region involved in turning devices on and off. This typically refers to metal-oxide-semiconductor (MOS) devices such as capacitors, field-effect transistors (MOSFETs), or insulated-gate bipolar transistors (IGBTs). All presented examples are from MOS gated SiC devices. Specifically covered is time-dependent dielectric breakdown (TDDB) testing, with either constant-voltage stress (CVS), constant-current stress (CCS) or ramped voltage stress (RVS) / ramped current stress (RCS) for ramped breakdown (RBD) tests.

An issue related particularly to SiC substrates is their high defect density; which has been rapidly decreasing over time as substrate quality improves, but remains orders of magnitude higher than for silicon substrates. This, and the resulting high interface trap levels present at SiO_2/SiC interfaces, has in the past interfered with the understanding of the intrinsic properties of SiO_2 on SiC. Thus, in the testing guidelines presented here, the intrinsic properties of the oxides on SiC are themselves important to demonstrate/determine. Extrinsic failures can often be related to intrinsic material defects in the SiC wafer material, or to processing issues, and any mathematical treatment of extrinsic defects is beyond the scope of this document. For detailed analysis of early fail populations (See JESD74A). Of course, the testing recommended here is to allow determination of the intrinsic and extrinsic populations, specifically through analysis of the failure distributions. However, the reasons for extrinsic failures, and means to eliminate them, are not addressed here, but helpful experimental procedures to analyze extrinsic failures will be described.

GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION PROCEDURES FOR SILICON CARBIDE POWER MOSFETS

(From JEDEC Board Ballot JCB-22-61, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

This document has two purposes; the first is presenting guidelines for the gate dielectric lifetime extraction and wear-out of MOS devices on silicon carbide substrates ("intrinsic behavior"). Specifically, it is designed for MOS devices (capacitors or transistors) where oxide thickness (t_{ox}) >> 10 nm. Therefore, 'soft' breakdown behavior is not expected to be observed, and oxide breakdown occurs instantaneously as a 'hard' breakdown event. Thus, issues relating specifically to thin oxides and soft breakdown are not addressed here. The second purpose is presenting guidelines for the measurement of gate dielectric breakdown, which are assumed to be defect related and occur much earlier than the wear out ("extrinsic behavior"). Although almost all data available in literature is on SiO_2 as a gate dielectric, the procedures outlined in this document apply to any dielectric layer. In case of a gate stack of different dielectrics, special care has to be taken when calculating the field distribution across the dielectric stack. This is not covered by this document.

MOS devices such as MOSFETs and IGBTs are designed to be operated at a fixed gate voltage (V_{GS}) level in the ON-state. As-such, oxide lifetime under controlled gate bias conditions is most appropriate for oxide lifetime extraction. On the other hand, charge to breakdown measurements or constant current stress can provide an alternative way to estimate lifetime, provided some conditions are fulfilled. Practical tests, which give oxide lifetime-related information, are (usually on-wafer and/or packaged devices):

- Constant-voltage stress (CVS) time-dependent dielectric-breakdown (TDDB) testing over short and relatively long time periods.
- Ramped-voltage stress (RVS) or ramped breakdown (RBD) approaches in which data for many samples can be obtained quickly. A voltage ramp is typically used for this test (V-Ramp), although a current, or current density ramp (J-Ramp), can be performed as well.
- Constant current stress (CCS) time dependent dielectric breakdown testing for low and high current densities.

It should be pointed out that all discussed tests provoke so-called hard-fails. This means that the device is typically "short" after the failure. "Soft" gate oxide failures (only a slight increase of the gate leakage current) as well as fails by parameter shifts were not expected in the typical gate oxide thickness range of SiC-based power-semiconductors. Furthermore, parameters like V_{TH} are typically shifting in such tests, but this is not a topic of interest in the evaluation of the tests.

Testing of gate oxide breakdown under accelerated bias, current or temperature conditions does not replace traditional qualification tests such as high-temperature gate bias (HTGB) testing called for in, for example, JESD22-A108F. This document is not meant to define acceptable lifetime limits, or proscribe acceptable use conditions; that is up to the device manufacturers and users.

2 Normative References

This guideline is meant to point out specific practices that may be applicable when testing gate oxide reliability for SiC-based power MOS devices. Practices proscribed in the following documents are to be followed, except where they are specifically modified in this present document:

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

JEP001A, *Foundry Process Qualification Guidelines* (2014).

JEP122H, *Failure Mechanisms and Models for Silicon Semiconductor Devices* (2016).

JESD35-A, *Procedure for the Wafer-Level Testing of Thin Dielectrics* (2001).

JESD35-2, *Test Criteria for the Wafer-Level Testing of Thin Dielectrics* (1996).

JESD47J.01, *Stress-Test-Driven Qualification of Integrated Circuits* (2017).

JESD91B, *Method for Developing Acceleration Models for Electronic Device Failure Mechanisms* (2022).

JESD92, *Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics* (2003).

3 Terms and Definitions

For the purposes of this publication, the following terms and definitions apply.

Terms in order of relevance:

TDDB: Time-dependent dielectric breakdown; most properly applies to conditions where all parameters are fixed except for time, but it is often applied to breakdown testing when other parameters are also varied (such as voltage or current) besides time.

CVS: Constant voltage stress; this is the typical TDDB condition, sometimes referred to as CV-TDDB to differentiate from ramped tests.

CCS: Constant current stress; is a TDDB condition in which the current density is kept constant during the duration of the stress.

RBD: Ramped breakdown; if voltage is ramped, it may be referred to as Ramped Voltage Stress (RVS), or V-Ramp; if current (or current density) is ramped, it is referred to as a Ramped Current Stress (RCS) or J-Ramp test.

3 Terms and Definitions (cont'd)

Defined variables in order of relevance:

t_{BD}: Time to breakdown (often units of seconds, or hours). The value t_{63} refers to the failure time for 63% of the devices (the Weibull alpha α), t_{50} refers to the time, at which 50% of the population fails (for lognormal distributions), etc.

t_{ox}: Oxide (or dielectric) thickness, measured electrically, optically, or physically.

V_{ox}: Voltage drop across oxide [V]

E_{ox}: Oxide field [V/cm], V_{ox}/t_{ox}. V_{ox} should be corrected for capacitor flatband voltage (V_{fb}) if V_{fb} is significant compared to V_{BD}.

V_{BD}: Oxide film breakdown voltage [V]

Q_{BD}: Charge to breakdown : t_{fail} x J_{dens} for a CCS experiment. J_{dens} is the current density during stress, t_{fail} is the time to failure.

4 Intrinsic G_{OX} Quality: Constant-Voltage Breakdown Stress

For SiC power MOS-based devices (MOS capacitors, MOSFETs, and IGBTs, for example), constant-voltage time-dependent dielectric breakdown (TDDB) testing should in most regards be consistent with the approaches established for silicon-based MOS devices in JEP001A for process qualifications, in JESD47J.01 for part qualifications, or as in JESD92 for characterizing gate oxide reliability and predicting lifetime, and JEP122H for mathematical description (models). Generally important aspects of testing are mentioned herein as guidelines for SiC power device testing.

JESD47J.01 recommends that either TDDB data or charge-to-breakdown data be available when new wafer fabrication or dielectric materials are utilized in a device family. General testing guidelines follow from JEP001 and JESD92. Because MOS devices are operated with a constant gate bias in the ON-state, constant voltage TDDB testing (time dependent dielectric breakdown, time-to-breakdown) is recommended for failure distribution and lifetime evaluation rather than constant-current testing (charge-to-breakdown). Although capacitor structures fabricated with the same processing as MOS transistors are allowed in other existing JEDEC documents, we recommend the testing of the actual product (i.e., transistors) where possible with positive polarity at the gate terminal (use case of the devices). Also voltage stress with negative polarity at the gate terminal should be considered if the devices are specified to have a negative gate voltage during turn-off.

4 Intrinsic Gox Quality: Constant-Voltage Breakdown Stress (cont'd)

If capacitors are used, they should be biased in accumulation, corresponding to the bias polarity used for the actual product. We want to point out that capacitor structures are less complex than transistors (in planar as well as in trench concepts) which may result in different, perhaps too optimistic experimental results.

The tested devices should be of large enough area to fairly represent product devices. We recommend measuring the biggest device in a device family which is expected to have the lowest lifetime in TDDB experiments due to the expected higher number of defects present in such devices, and to carry out investigations on area scaling whenever necessary.

4.1 Experimental Procedure in General

As a prerequisite, comparable groups of devices (same product type, same specification, standard production) should be chosen. Continuous monitoring of gate leakage (for CVS) or of voltage (for CCS) across the gate dielectric is the preferred way to determine failure time. Known good devices are selected for the test. The time to breakdown for each device at the V_{GS} stressing value (constant voltage stress). The failure criteria must be consistent; typically a leakage current value or a current increase rate (or a drop in V_{GS} if V_{GS} is being monitored). Issues mentioned in JESD92 Annex A should be considered regarding the measurement and instrumentation requirements. The number of devices tested per stress condition should be at least 25 devices.

4.2 Constant-Voltage Breakdown Stressing at High Electric Fields

At high electrical fields the failure mechanism is expected to change during the experiment, and the observed parameters are not valid for lifetime extrapolation. Such experiments can be performed either on wafer material or with discrete packaged parts. The derived failure distribution can typically be separated in an intrinsic and an extrinsic part and allows conclusions on electrical defect density. The observed β-values may not be representative of low-field behavior due to additional failure mechanisms which become active at high fields, but the results of high-field testing are sufficient to compare different process variations. Also the t_{63}/t_{50}-values can be used for process comparisons. Contrary, the observed γ–values are typically very high and an extrapolation to lower electrical fields would likely lead to wrong results.

At high electrical fields, failure of the dielectric is due to positive charge trapping. Typically this occurs for E_{ox} >8 MV/cm at room temperature, and E_{ox} >9 MV/cm at T = 175 °C. A practical way to assess if one is in the positive charge trapping regime, is by inspecting the I_g-t (for constant voltage stress) or V_g-t (for constant current stress) curves. If I_g increases as a function of stress time (or V_g decreases), one is under the "high field" stress condition.

4.3 Constant-Voltage Breakdown Stressing at Low Electric Fields

Parameters of such experiments (described by the t_{63}/t_{50}, β, γ) are suited for lifetime extrapolation towards typical use fields. Such experiments are typically carried out by testing of discrete packaged parts in an oven because this setup allows long stress times (hundreds of hours, even 1000 hrs or 2000 hrs). The derived failure distribution can also typically be separated in an intrinsic and an extrinsic part and allows conclusions on electrical defect density.

At low electrical fields, failure of the dielectric is due to negative charge trapping. Typically this occurs for E_{ox} <8 MV/cm at room temperature, and E_{ox} <9 MV/cm at T = 175 ºC. A practical way to assess if one is in the negative charge trapping regime, is by inspecting the I_g-t (for constant voltage stress) or V_g-t (for constant current stress) curves. If I_g decreases as a function of stress time (or V_g increases), one is under the "low field" stress condition. An example is given in Figure 10.

4.3.1 Product Quality Testing

For a representative product family, at least 3 representative groups of parts (typically ≥25 or more parts/group) should be stressed at different $V_{GS(stress)}$ values greater than V_{GS}(use), and held until approximately 63% of the population fails. Then a field acceleration parameter (γ) can be calculated for lifetime determination at the use voltage. Ideally all parts should be taken to failure, or at least one of the 3 populations (for a complete failure distribution determination). If V_{GS} values have been appropriately chosen, all failures should occur within the ranges of hours to a thousand hours. If all parts in all 3 populations fail in less than 10 hours, then the voltage levels chosen are too high, and this may not properly provide true lifetime extrapolation. Ideally these tests are performed at the device maximum rated use temperature, as it is known that failure rates of SiO_2 (and oxide dielectrics in general) increase with increasing temperature. It is recommended to have all parts under test held in an oven for temperature uniformity.

A Weibull plot of percent failure versus time will give the Weibull slope beta (β) for each population, and the measured t_{63} is the Weibull scale parameter alpha (α). For product quality testing, Weibull slope value β, and projected lifetime for the t_{63} or t_{50} failure percentages at the V_{GS}(use) value using the linear field E-model, are recommended as quality metrics. Since the intrinsic Weibull slope β is a characteristic of the dielectric under stress, it should be independent of the stress condition and hence all failure data should be fitted with one intrinsic Weibull slope (and not a different Weibull slope per individual stress condition).

As per the field acceleration model, different models exist in literature (E-model, 1/E model, V^n model). It is recommended to use the most conservative model (E-model) unless that data unambiguously points to another field acceleration model.

4.3.2 Lifetime Testing

For a complete intrinsic lifetime determination, parts should be tested at various temperatures, such as room temperature (25°C) and the maximum allowed operation temperature, and preferably a 3rd temperature (either intermediate or somewhat higher than the maximum allowed use temperature). The maximum allowed temperature has to be tested in any case. As mentioned in the previous subclause, at least 3 groups of parts (with typically ≥25 or more parts/group) should be stressed at V_{GS} values greater than V_{GS}(use), and held until at least 63% of the population fails, for each temperature. Outliers (extrinsics; i.e., measurement values significantly deviating from the intrinsic Weibull data fit) should be excluded. To determine if a part belongs to the intrinsic distribution or not, 95% confidence levels can be used.

Then a temperature-dependent field acceleration parameter or an apparent activation energy can be calculated, to allow lifetime determination at the use voltage for a range of temperatures. Ideally all parts should be taken to failure for at least one of the populations at each temperature. If V_{GS} values have been appropriately chosen, all failures should occur within the ranges of hours to a thousand hours. If all parts in all 3 populations fail within, or close to, 10 hours, then the voltage levels chosen are too high, and this may not properly provide true lifetime extrapolation. Parts for package level tests are held in an oven to maintain uniform temperature ambient. The same can be achieved for wafer level tests via a thermo chuck.

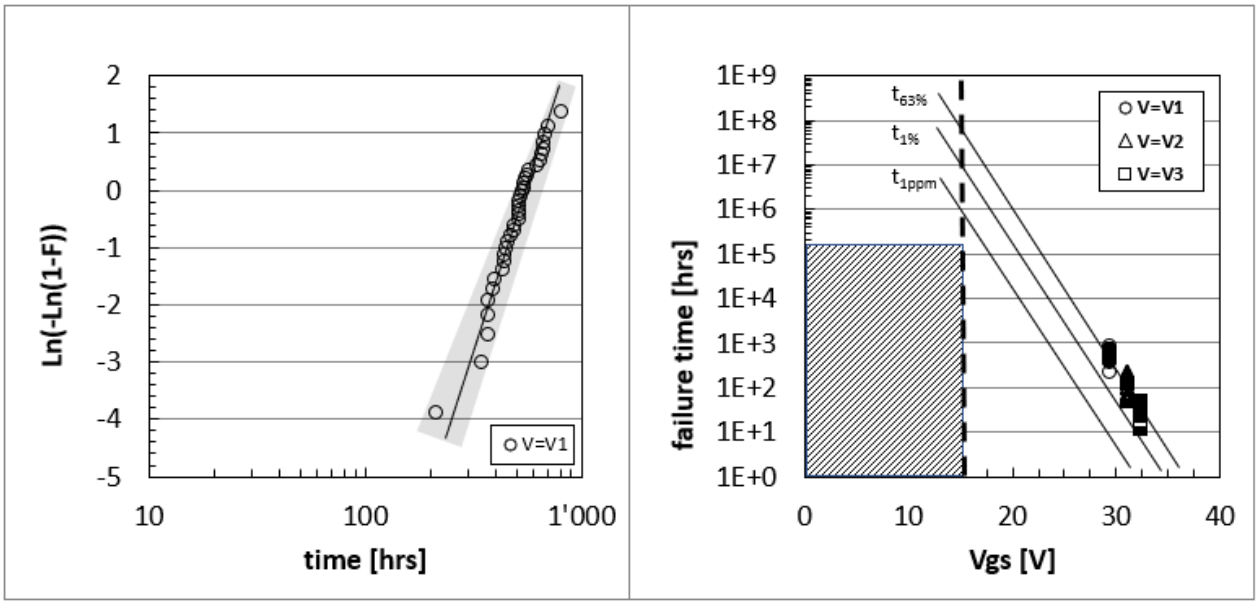
A Weibull plot of percent failure versus time will give the Weibull slope β for each population, and the measured t_{63} is the Weibull scale parameter α. From the t_{63} time for each of the 3 populations (or another representative time such as t_{50}), a plot of ln(t_{BD}) versus V_{GS} can be used to extrapolate lifetime to the use V_{GS} value (for at least 3 populations measured at a fixed temperature). This type of extrapolation presumes that the linear field model (E-model) is the appropriate model to determine lifetime. Although some debates exist concerning appropriate lifetime modeling, it is recommended to use the "Linear-E-model" as it gives a slightly more conservative lifetime prediction than other approaches and is simple to apply. This is especially the case for devices with thick gate oxide layers (>20 nm). Power law extrapolation or other mathematical approaches should only be used if they could be experimentally verified; in case of their use the lifetime extrapolation method should be clearly stated.

When measurements are performed at multiple temperatures, the representative t_{BD} for each population (t_{63} or t_{50}) at the given temperature can be plotted versus inverse temperature, and the effect of temperature on lifetime will be shown. The effects of temperature can be lumped into the field acceleration parameter, or listed as an apparent activation energy, depending on the mathematical approach used (See subclause B.3).

In summary, CVS TDDB data is best displayed by:

1) Weibull plots showing the failure distribution at a given temperature and V_{GS} condition, with the Weibull slope β calculated by fitting the majority of the distribution (this focusses on the intrinsic population).
2) Lifetime plots extrapolating the failure time (t_{63}, t_{50}, or other representative failure percentile such as t_1) to the use voltage, preferably plots of ln(t_{BD}) versus V_{GS} fit using a straight line in the case of the E- model to obtain failure rates at the V_{GS}(use) value. Other lifetime extrapolation methods can be used, as long as the approach is clearly defined and experimentally verified.

4.3.2 Lifetime Testing (cont'd)



NOTE 1 This example TDDB Weibull failure distribution is for parts held at one stress condition including fit line and 95% confidence level (left), and failure time extrapolation for 3 groups of stressed parts, using a straight line to fit the 63%, 1%, and 1 ppm failure populations (right). From the lifetime plot, estimated lifetime at any given V_{GS} value can be obtained (at that measurement temperature).

NOTE 2 Exemplarily, a potential device specification of 15 V/20 y was added in the figure on the right side.

Figure 1 — TDDB Weibull Failure Distribution

5 Inline Monitoring of Process Quality by Ramped Breakdown Testing

To get a fast estimation of the gate oxide defect density, one can use ramped voltage or ramped current approaches (termed V-Ramp and J-Ramp in JESD35A). These tests are typically carried out in a way that the tested devices are stressed to failure/breakdown (end-of-life test). Both methods are faster and simpler than traditional TDDB measurements. As such, they can be very useful for process control monitoring. In principle they can also be used for lifetime extrapolations (See [5], [6] and subclause B.5), although some debate remains as to whether it gives predictions equivalent to TDDB testing. Thus, TDDB is the recommended test for lifetime evaluation, but the V-ramp technique is probably a more useful technique for quickly monitoring oxide quality with high statistics.

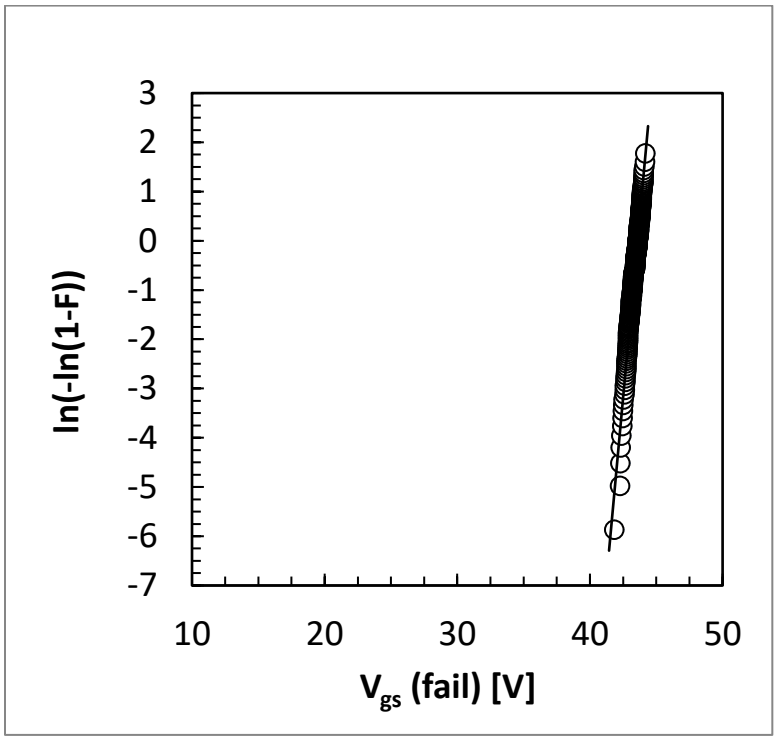
Ramped breakdown testing is usually performed (inline, after wafer processing) on a (semi-) automatic probe station with a heated chuck, such that testing of many dies on a wafer can be automated. Typically a pretest of I_{GS} is performed at $V_{GS}(use)$ before the voltage is ramped from a level below $V_{GS}(use)$ until the breakdown occurs. As in TDDB, breakdown is defined by reaching a given current level or a current increase above a certain rate. It is desirable to maintain the complete set of I_g-V_g data in order to plot the data and extract Fowler-Nordheim dielectric/SiC barrier height for the product being measured, and to document how the breakdown event proceeds.

The voltage step size of the ramp should be small enough to obtain a V_{BD} value allowing good resolution of the failure voltage for each part, such as a voltage step which is <1% of the V_{BD} for that product. The total ramp rate should be moderate and within the capability of the measurement setup. It should not be too fast (e.g., steps in the low ms or µs-range) as not to reach significantly higher VBD values as in the TDDB test thereby invoking other (high-field) failure mechanisms (observing the same failure mechanism as measured in TDDB is the goal of this test). The ramp rate should be such that t_{BD} is at minimum greater than about 10 seconds for a given ramp rate, to not compromise accuracy and repeatability.

For process quality monitoring, testing of a (randomly selected) population of ~100 parts (die, or on-wafer) is typically sufficient. If failure probabilities in the 1% range or lower are of interest, it is recommended to measure much more than 100 parts. This is the principal reason to use the V-Ramp approach, to measure large numbers of samples quickly. For this, a single ramp rate (giving a reasonable failure time resolution) and a single temperature (ideally the device rated temperature) can be used.

To test gate oxide defect density that is independent of device structure (e.g., quality of the oxidation or deposition process), large MOS capacitors are very appropriate to use. From this test, a failure distribution plot on a Weibull scale versus the VBD gives the pertinent information regarding the oxide properties of the population tested (Figure 2). Here the Weibull parameter α gives the breakdown voltage 63% failure quantile, and the slope is a measure of oxide quality (but is not the same as the Weibull slope for TDDB measurements versus time).

5 Monitoring of Process Quality by Ramped Breakdown Testing (cont'd)



NOTE This is an example of ramped breakdown failure points (Vgs at failure) for a group of 250 large area capacitors taken to breakdown.

Figure 2 — Ramped Breakdown Failure Distribution for Large-Area Capacitors

The defect density level of the process can also be analyzed. For this purpose, fully processed devices need to be used and the sampling has to be chosen adequately. Extrinsic devices can be observed as devices with VBD breakdown values deviating from the Weibull failure distribution (See JESD35A, subclause A.2). It is expected that they are the result of defects in the gate oxide or local oxide thinning. For further root cause analysis, methods of the physical failure analysis can be used.

The transition from extrinsic to intrinsic data points within a failure distribution is indicated by an inclination point which discriminates between the measured devices with an intrinsic and an extrinsic failure mechanism. Even if it is quite straightforward to estimate the total (extrinsic) defect density, it is much harder to determine whether an extrinsic defect (that fails at a somewhat lower V_{BD}-value) is actually critical for the application, i.e., if the affected device would fail during the aspired device lifetime or not. Additional analysis techniques and other test setups have to be considered for that.

6 Accompanying Tests on Gate Oxide Defects and Extrinsic Gate Oxide Quality

In this chapter, methods are described to analyze and compare the gate oxide properties of different SiC MOSFET groups, e.g., from different technology nodes or different manufacturers.

As a prerequisite SiC MOSFETs have to be used which are representative for the typical outgoing quality of the particular manufacturer, and have been exposed to all prescribed tests by the manufacturer (optical inline inspections, electrical tests and screening, burn-in etc.).

6.1 Test Procedure: Step-Wise Increased Gate Voltage

In this subclause, a test procedure to compare extrinsic and intrinsic gate oxide properties of different SiC MOSFET devices will be discussed. The test is based on a stepped gate voltage sequence, which is performed at elevated temperature [2], [4]. To perform the test, only some basic datasheet values need to be known:

- The recommended gate use voltage ($V_{G,use}$), the maximum allowed gate use voltage ($V_{G,max}$), and the recommended use temperature (T_{use}).
- An ensemble of SiC MOSFET devices, e.g., 100 parts, is pre-characterized at room temperature. For instance, gate integrity is measured.

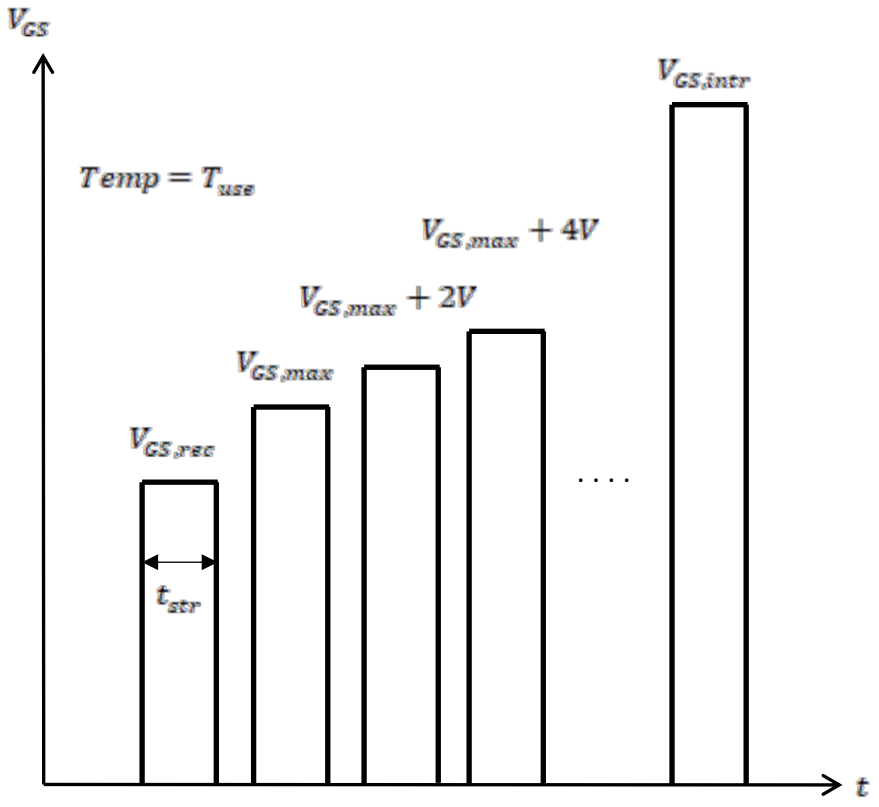


Figure 3 — Proposed Gate Voltage Step Test Sequence.

6.1 Test Procedure: Step-Wise Increased Gate Voltage (cont'd)

Referring to Figure 3, before and after each stress sequence, the gate integrity of each chip is checked via an IGSS (gate-source leakage) test. The procedure is an end-of-life test.

In a first stress step, all devices are stressed at the temperature T_{use}, e.g., 150°C, for a time t_{str} at the recommended gate use voltage $V_{G,use}$. After stress, all devices are checked for IGSS (gate-source leakage current) failures. An appropriate stress time t_{str} could be 18h so that one cycle of stress and measurement could be carried out in 1 day. Also, longer stress times like 168 hrs could be chosen. Devices which failed during step 1 are counted and removed from the distribution. The second stress step is performed in the same way but at the maximum allowed use voltage $V_{G,max}$. Devices which failed during step 2 are again counted and removed from the distribution. The test is continued in this way with gradually increasing stress voltage, e.g., by +2 V after each stress step, until all devices have failed. Also, other voltage step sizes could be chosen, but it is advised to use roughly 20-30 equidistant steps between $V_{G,use}$ and V_{BD} (V_{BD} should be determined beforehand in a fast voltage ramp experiment).

At the end of the test, the failed devices after each stress step are analyzed in a Weibull plot.

Experimentally, the CDF can be determined using Bernard's approximation:

$$F_i = \frac{i-0.3}{N+0.4} \tag{1}$$

where i is a running index indicating the number of failed devices and N is the total number of tested devices. The y-axis of the Weibull plot is calculated by linearization of the cumulative density function (CDF)

$$ln(-ln(1-F_i)) = \beta \cdot ln\left(\frac{t_{use}}{\tau}\right) \tag{2}$$

Using the linear E-model, the life time (typically the x-axis of the Weibull plot) can be expressed as a function of the difference $V_{G,str} - V_{G,use}$ for an extrinsic spot with an electrical oxide thickness d'_{ox}

$$t_{use} = t_{str} exp\left(\frac{\gamma}{d'_{ox}}\left(V_{G,str} - V_{G,use}\right)\right) \tag{3}$$

d'_{ox} is related to the stress time (t_{str}) and the stress voltage ($V_{G,str}$) at which the defective device fails. E_{BD}^{1h} is the value for the electrical field at which a typical intrinsic breakdown occurs after 1 hour:

$$t_{use} = t_{str} exp\left(\left(\gamma E_{BD}^{1h} - ln\left(\frac{t_{str}}{3600}\right)\right)\left(1 - \frac{V_{G,use}}{V_{G,str}}\right)\right) \tag{4}$$

$$ln\left(-ln(1-F_i)\right) = \beta\left[ln\left(\frac{t_{str}}{\tau}\right)\right] + \beta\left(\gamma E_{BD}^{1h} - ln\left(\frac{t_{str}}{3600}\right)\right)\left(1 - \frac{V_{G,use}}{V_{G,str}}\right) \tag{5}$$

6.1 Test Procedure: Step-Wise Increased Gate Voltage (cont'd)

In the double logarithmic ordinate (y-axis) representation, the Weibull distribution described in the equation above shows a *linear* increase over time if one minus the ratio of use and stress voltage is chosen as the abscissa (x-axis). Note that the slope depends only on material parameters and on the stress cycle time. The constant term in the last equation includes the scale parameter τ which is dependent on the extrinsic defect density.

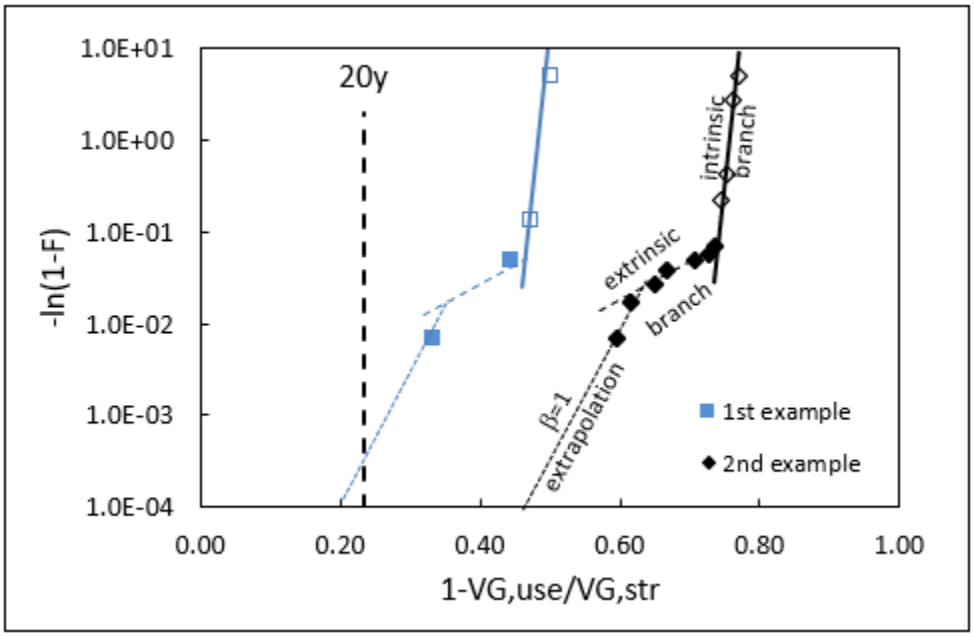
Figure 4 shows exemplary the failure probability of the experimental results for two different groups consisting each of 100 SiC MOSFETs. From the number of failures after each stress step a Weibull plot was created based on the above formulas. Intrinsic and extrinsic parts of the distributions can be distinguished by the slope (c.f. Figure 4).

Often one can observe two different extrinsic slopes in the Weibull plot, the first being close to $\beta = 1$ while the second has a $\beta < 1$. This behavior is typically due to an electrical screening or a burn-in that was performed prior to this test. Electrical screening or burn-in cuts-off early failures from the original extrinsic distribution and leads to a constant failure probability with $\beta = 1$ for some time in any subsequent gate-oxide reliability experiment [1]. The location on the x-axis where the $\beta = 1$ slope turns into a $\beta < 1$ slope is a measure of the sharpness of the electrical screening or burn-in that was performed prior to this test. Failures that occur before this point may be extrapolated back using a $\beta = 1$ slope. The location on the x-axis where the $\beta < 1$ slope turns into a $\beta > 1$ slope marks the onset of intrinsic failures and is therefore a measure of the bulk oxide thickness and quality. Also, a comparison of these failure probabilities to the total life time (e.g., 20 years) can be carried out by calculating the equivalent stress voltage to the specified use voltage for one stress cycle.

It has to be mentioned that the sample size used in this test needs to be adjusted to the extrinsic defect density of the tested device technology in order to learn something about the extrinsic gate oxide quality. If the sample size is chosen too small so that no early failures are observed during the test, the output of the experiment is limited to the information on the intrinsic failure branch, and hence, the bulk oxide thickness and quality. In this case no statement on the extrinsic gate oxide quality can be made besides the obvious conclusion that the extrinsic defect density is smaller than the tested sample size.

The advantage of this procedure is that it is a straight-forward end-of-life method that tests the entire bath-tub curve, thereby providing a complete picture of extrinsic and intrinsic gate oxide quality, the resolution of the former being only limited to the tested sample size.

6.1 Test Procedure: Step-Wise Increased Gate Voltage (cont'd)



NOTE This chart is a symbolic illustration of a Weibull plot of intrinsic and extrinsic failure rates for different SiC MOSFET devices. The open symbols correspond to devices which break down intrinsically. The full symbols correspond to devices with break down extrinsically. The dashed lines indicate the extrinsic branches, the straight lines the intrinsic branches. The target chip life time of 20 years is indicated as vertical dashed line. The line can be understood as the required stress voltage applied for one stress cycle, which represents the use voltage applied for 20 years.

Figure 4 — Weibull Plot of Intrinsic and Extrinsic Failure Rates for Different SiC MOSFET Devices

6.2 Test Procedure: Early Life Failure Test by Soft Overstress on a High Number of Samples (Marathon Test)

In this subclause a test procedure to analyze extrinsic properties of SiC MOSFET devices (including the early failure rate) will be discussed (See [1]). As already stated at the end of the previous paragraph, the key to quantify extrinsic failure probabilities is to test large sample sizes. Assuming a population of devices with 1% extrinsic failures in the gate oxide screening, one needs to test a large number of parts (on the order of 1000 devices) in an accelerated stress test to catch enough remaining extrinsics for a meaningful evaluation of the "post-screening field-failure probability".

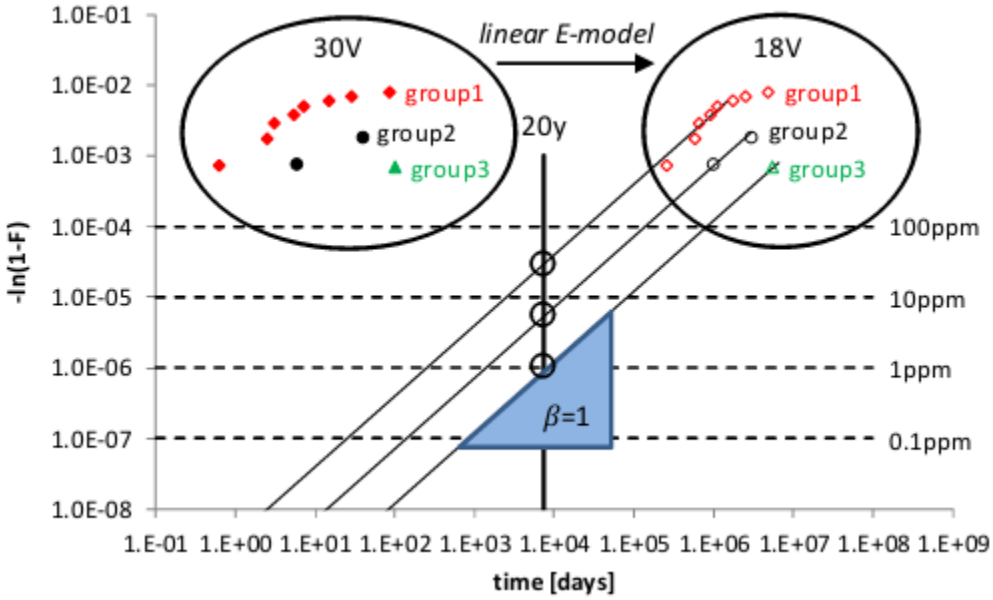
For this purpose, a large number of samples is stressed in a parameter range (voltage, temperature) comparable to typical burn-in conditions. Contrary to burn-in, a much longer stress-time (e.g., 1 e^{+7} s) is used.

6.2 Marathon Test (cont'd)

The gate bias levels should be chosen far below the intrinsic wear-out regime and therefor intrinsic failures will not be observed during the experiment. But the stress conditions should be still harsh enough to trigger a few failures within the duration of the test.

The time to failure (TTF) distribution at stress voltage can be converted to a TTF at use voltage by using an appropriate lifetime extrapolation model (e.g., Linear E-model). It is proposed to use the same model and model parameters for all data points, i.e., intrinsic and extrinsic data points. This is equivalent to the understanding that extrinsic fails (early fails) are either provoked by a local oxide thinning, or another different failure mechanism can at least be described similarly by a locally thinner gate oxide.

In this way it can be determined whether the observed failures at stress conditions would have occurred at use conditions during the specified product lifetime or afterwards. Extrinsic failures that occur after the specified product lifetime are uncritical for the application. However, these data points are important as they can be used to extrapolate the Weibull plot back to the real product lifetime and in this way estimate an extrinsic lifetime failure probability (See Figure 5). If a burn-in or a voltage screening was done prior to the Marathon-Test, first extrinsic failures are expected to come with a Weibull slope close to $\beta = 1$ indicating a constant failure probability over time. The linear slope after burn-in or voltage screening is also here due to the elimination of early failures up to a certain point in the bath-tub curve. In this case extrapolation back to product lifetime at use conditions shall be done using a Weibull slope of $\beta = 1$.



NOTE This example is for an assessment of the failure probability of 3 different groups of SiC MOSFET samples. Measurements were carried out at 30 V, and then the data were recalculated to use conditions (here: 18 V) by using a physical model. $\beta = 1$ was used to extrapolate the distributions to lower failure probabilities.

Figure 5 — Failure Probability of Three Different Groups of SiC MOSFET Samples

Annex A (Informative) Current Based Methods

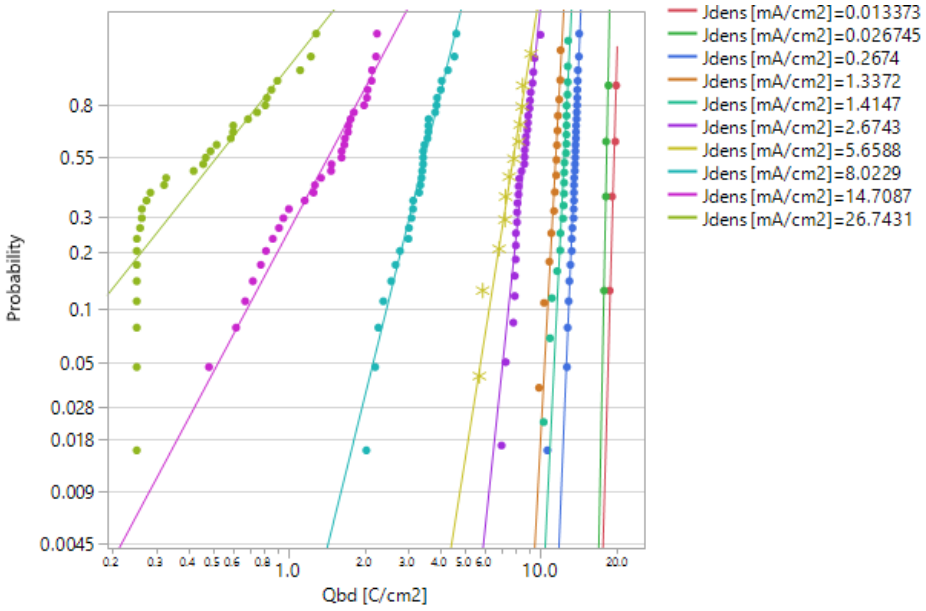
Constant Voltage Stress TDDB, as described in 4.3, is widely used in the industry to assess dielectric lifetime. The drawback of CVS TDDB is that the field acceleration model is not a priori known (hence the suggestion to use the "most conservative" model), and the fact that the Weibull slope β is too low to be consistent with theoretical predictions for thick oxides.

An alternative methodology to assess the lifetime of SiC capacitors and MOSFETs is to use a current-based approach, in which the devices are stressed at different stress current densities J_{dens} (expressed in A/cm^2) instead of different gate voltages. It is insensitive to variations in the oxide thickness, but Weibull slopes are typically larger than in CVS-TDDB (variations in oxide thickness within the test group leads also to variations in the electrical field). The parameter that is monitored is Q_{BD} (expressed in C/cm^2), which is calculated from t_{fail} according to equation A.1. In case of planar MOSFETs the area is the total gate area, including the channel and JFET gate overlapping area.

The methodology could also be applied to trench devices or devices with non-planar topography, but then especially the corners would have a much larger impact and normalization to the device area could not be performed in an easy way.

$$Q_{CRIT}\left[\frac{C}{cm^2}\right] = J_{DENS}\left[\frac{A}{cm^2}\right] \times t_{fail}[\mathrm{s}] \qquad \text{(A.1)}$$

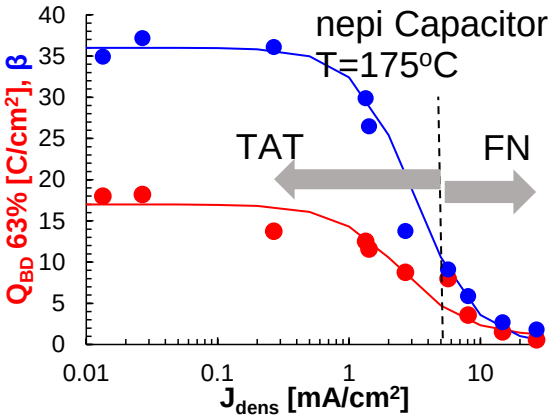
For each J_{dens}, a minimal sample size of 25 devices is recommended. The obtained Q_{BD} data are plotted on a Weibull plot. See Figure 6 for a typical example. Figure 7 plots the Q_{BD} at 63.2% of the failure population, as well as the Weibull slope β versus J_{dens}.



NOTE This Weibull plot is of Q_{BD} from constant current stress at T = 175 °C for different stress current densities, on n-epi SiC capacitors with t_{ox} = 53 nm. For the highest stress current densities, the data is not Weibull but lognormal (See [3]).

Figure 6 — Weibull Plot of Q_{BD} from Constant Current Stress

Annex A (Informative) Current Based Methods (cont'd)



NOTE This Weibull analysis uses the Q_{BD} data of Figure 6; constant current stress at T=175 °C for different stress current densities. For low stress current densities, a constant "critical" charge density Q_{CRIT} is reached, with a high Weibull slope β.

Figure 7 — Weibull Analysis of Q_{BD} from Constant Current Stress

Inspecting Figure 6 and Figure 7, two important experimental observations can be made (See [3]). Depending on the applied stress current density J_{dens} there are two distinct regions in the Q_{BD} versus J_{dens} plot:

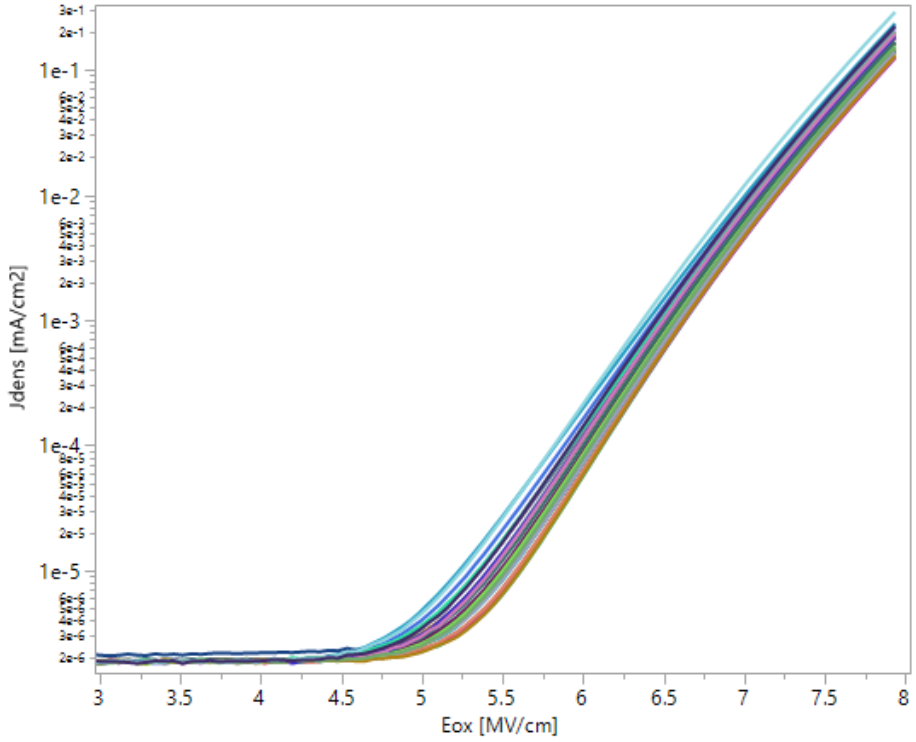
1. For low J_{dens} Q_{BD} is Weibull distributed, with a steep Weibull slope β. This is the regime where negative charge trapping prevails and where the current transport through the dielectric is by trap-assisted tunneling (TAT). Monte Carlo modeling for neutral defect formation or negative charge trapping predicts a Weibull slope of 41, for a 50 nm thick oxide. For high J_{dens} Q_{BD} is lognormal distributed (reflected by a poor Weibull slope). In this case, current transport through the dielectric is by Fowler Nordheim tunneling (FN) and positive charge is stored.
2. For low J_{dens} a critical charge-to-breakdown "Q_{CRIT}" exists for which the dielectric fails. In the case of the data of Figure 12, Q_{CRIT}~15 C/cm^2 for J_{dens} <1 mA/cm^2, with a corresponding β ~30. Q_{CRIT} is a unique characteristic for a given process technology and is clearly Weibull distributed with a steep Weibull slope. Hence, Q_{CRIT} can be calculated at any given failure rate or ppm level using the Weibull failure function. At higher J_{dens}, Q_{BD} drops to much lower values, since positive trapping leads to current focalization resulting in a lower Q_{BD} and a lognormal distribution, as predicted by Monte Carlo modeling.

It is mandatory that Q_{CRIT} is extracted for low enough stress current densities, where the dielectric fails due to negative charge build-up. Otherwise, the failure mechanism would be different compared to application conditions at low electric fields. Q_{CRIT} is dependent on temperature and decreases with increasing temperature. Hence, Q_{CRIT} is to be determined at the highest rated temperature.

Annex A (Informative) Current Based Methods (cont'd)

The fact that for low J_{dens} stress conditions the devices fail for a given critical charge Q_{CRIT} can be used to estimate the lifetime of the dielectric by using equation A.1. Note that unlike standard constant voltage gate TDDB, no field extrapolation is required since the field dependency is implicitly contained in the measured gate current characteristic. In other words, if current (or charge) is the determining factor for dielectric lifetime, the I_g-V_g characteristic in itself contains the field acceleration, which can be directly derived from the experimental I_g-V_g characteristic.

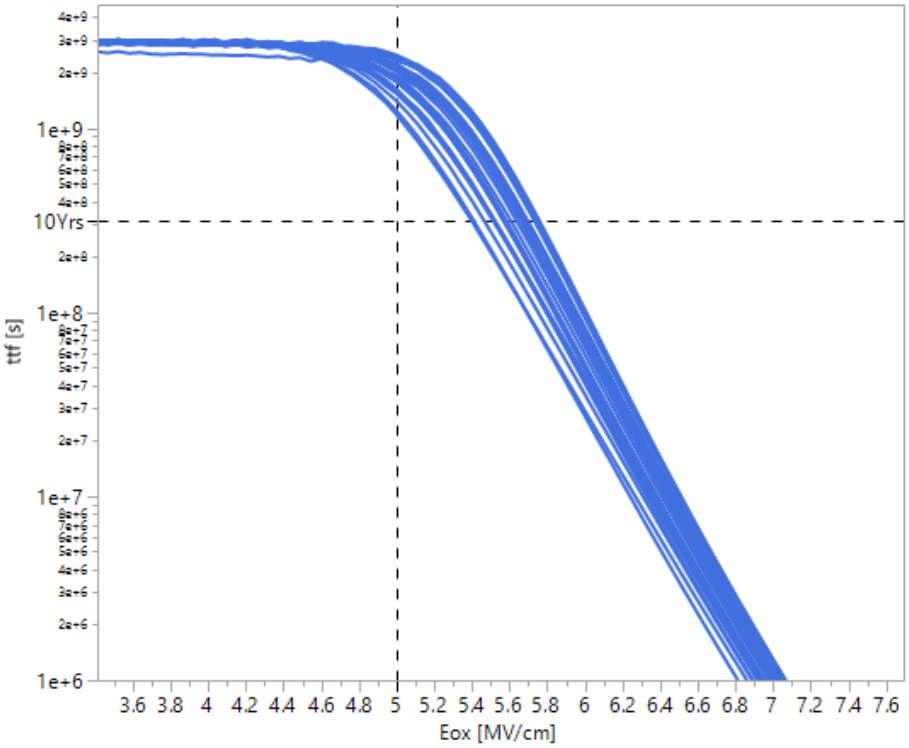
Figure 8 shows an ensemble of 30 J_{dens}-E_{ox} characteristics, measured at T = 175 ºC. The resulting estimated t_{fail}, assuming a Q_{CRIT} = 5.5 C/cm^2 at 100 ppm, using equation A.1 is plotted in Figure 9. For E_{ox} <5 MV/cm, the resolution of the measurement caps the lifetime. However, the analysis of this example indicates that the intrinsic lifetime of the dielectric is larger than 10 years, at 5 MV/cm, at 100 ppm at T = 175 ºC. This is consistent with constant voltage stress TDDB data performed on the same gate oxide.



NOTE T = 175 ºC, sample size is 30.

Figure 8 — J_g-V_g Characteristics of n-Epi Capacitors, Mapped Across Different Wafers

Annex A (Informative) Current Based Methods (cont'd)



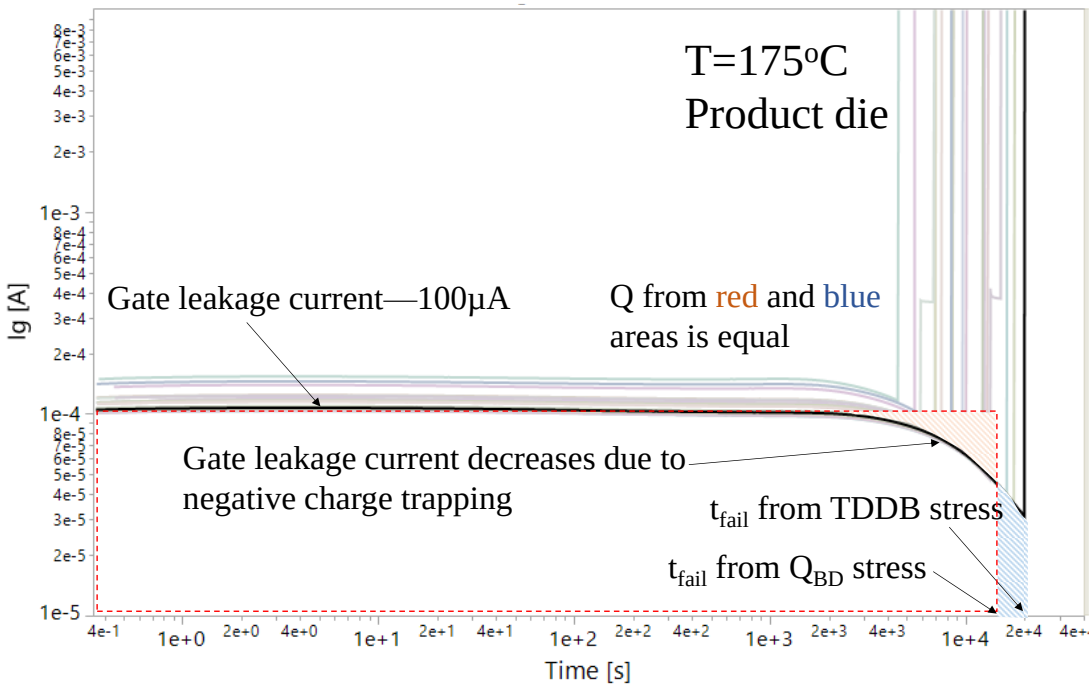
NOTE The lifetime estimate is of the n-epi capacitors from Figure 8 at T = 175 °C, at 100 ppm failure. Q_{CRIT} is taken from the Weibull data of Figure 7.

Figure 9 — Lifetime Estimate of n-Epi Capacitors

A potential drawback of any current based approach is that the gate of a transistor under typical operation is voltage driven rather than current driven. As such, a constant current experiment would not represent true life operation. However, the gate voltage can easily be measured during constant current stress to convert the current density into gate voltage level, that is, however, not constant during the test.

Annex A (Informative) Current Based Methods (cont'd)

Figure 10 shows the variation of the gate current I_g during a constant voltage TDDB experiment, for an ensemble of 30 SiC MOSFET transistors, at T = 175 °C. All behave similarly. As an example, the I_g of one device is highlighted (full black curve).



NOTE The constant voltage TDDB experiment is for low E_{ox} (negative charge trapping regime). Experiments were done on planar MOSFET transistors stressed in accumulation, T=175 °C. The current through the dielectric remains constant for many decades of stress time and decreases before the failure point.

Figure 10 — I_g Versus Time During a Constant Voltage TDDB Experiment

For the MOSFETs of Figure 10, when applying a constant voltage stress at low enough stress field, I_g remains constant for many decades of stress time, and I_g drops prior to the failure point due to negative charge trapping. This is the failure mode that will occur during normal operation of the device. As can be noticed from Figure 10, there will be no difference between a constant voltage or constant current stress, for the first ~2 e^{+3} seconds of stress time since I_g remains constant. When negative charge trapping sets in, the current through the dielectric stack will decrease. This means that the time to reach a given charge budget Q_{CRIT} will increase. In other words, the time-to-fail will be postponed and the device will fail later than when a constant current stress at 100 µA would be applied (at 2 e^{+4} seconds in the example of Figure 10), which would be around 1.2 e^{+4} seconds.

t_{fail} from TDDB will be such that the blue and red shaded areas are equal, but will always be larger than t_{fail} from Q_{BD}. Hence estimating lifetime from Q_{BD} will be an underestimation of the true lifetime ("conservative approach').

Annex B (Informative) Supplemental Data Analysis

B.1 Failure Distributions

Oxide failure distributions are best modeled using Weibull statistics (JESD122H, JESD92). The Weibull cumulative distribution function (CDF) or unreliability function:

$$F(t) = 1 - \exp[-(t/\alpha)^{\beta}] \quad \text{(B.1)}$$

The Weibull slope (β) represents the tightness of the failure distribution, and shape factor (α) represents the t_{63} failure time. These are obtained by plotting $\ln(-\ln(1-F(t)))$ versus $\log(t_{BD})$.

B.2 Area Scaling

The Weibull slope is used for area scaling, and the time to breakdown (t_{BD}) scales with area as:

$$t_{BD1}/t_{BD2} = (A_2/A_1)^{1/\beta} \quad \text{(B.2)}$$

where A_1 and A_2 represent the areas of devices 1 and 2, β is the Weibull slope of the failure distributions, and t_{BD1} and t_{BD2} are the representative failure times (such as t_{63}) of each device population (See JESD92).

B.3 Lifetime Extrapolations

Oxide lifetime extrapolations are most conservatively modeled using the linear E-model (or thermochemical model), commonly expressed as:

$$t_{BD} = \tau_0(T)*\exp(-\gamma(T)*E_{ox}) \quad \text{(B.3)}$$

where the prefactor (τ_0) and the field acceleration parameter (γ) are temperature (T) dependent;
or

$$t_{BD} = A_0*\exp(-\gamma(T)*E_{ox}) *\exp(E_a/kT) \quad \text{(B.4)}$$

where the prefactor (A_0) is a scaling constant, and the apparent activation energy (E_a) is in units of [eV]. The field parameter $\gamma(T)$ is observed to scale inversely with temperature for silicon-based MOS devices. The field parameter γ units are properly written as ‘Naperians/MV/cm’ when extracted using the natural logarithm, and as ‘Decades/MV/cm’ when extracted using the base-10 logarithm; the latter giving a γ value 2.303 times smaller.

See JEP122H and JESD91B for more detail regarding the temperature dependence of the field parameter, and the field dependence of the activation energy, and details of the 1/E model and other related models.

B.4 Ramped Gate I_G-V_G and Fowler-Nordheim Tunneling

A good quality check of the gate oxide dielectric properties is to analyze the leakage current and to see if it fits the expected FN tunneling behavior. This ensures that defect-assisted leakage mechanisms are not dominating the dielectric properties, which would limit dielectric lifetime. The FN leakage current density (J_{FN}) is given by:

$$J_{FN} = A*E_{ox}^2*\exp(-B/E_{ox}) \quad \text{(B.5)}$$

where:

$A = 1.54 \times 10^{-6}*(m/m_{ox})*(1/\Theta_B)$ in A/V^2, and
$B = 6.83 \times 10^{-7}*(\Theta_B^3*m_{ox}/m)^{1/2}$ in V/cm.

Here m is the free electron mass, m_{ox} is the electron (or hole) mass in the oxide, and Θ_B is the effective FN barrier height. For an N-type capacitor biased into accumulation, the electron effective mass (~0.42 eV) is used, and the conduction band FN barrier height is measured. A plot of $\ln(J_{FN}/E_{ox}^2)$ versus $1/E_{ox}$ (a FN plot) gives an intercept of A and slope of B. From the slope B, the effective barrier height Θ_B can be extracted. A quality SiO_2 film on SiC should be linear on a FN plot in the FN leakage region, and give a FN barrier height Θ_B of about 2.8eV. This also helps to verify the oxide field values (See JESD92 and JESD35A).

FN current is typically higher for SiC based devices than for similar Si based devices.

B.5 Ramped Gate Lifetime Extraction

Lifetime extrapolation is best done using typical constant-voltage TDDB testing. Using V-Ramp data for lifetime determination can also be an approach used to compare oxide processes to one another. As with TDDB, this would require measurements to be performed using at least 3 different ramp rates (analogous to TDDB at 3 different V_{GS} values) for field acceleration parameter determination. If desired, multiple temperatures can be used for determining temperature acceleration (activation energy). Ideally, to demonstrate the accuracy of extrapolating lifetime using V-ramp data, one set of TDDB data at the same temperature should be available for comparison of the field acceleration parameter. After that, the V-Ramp data at multiple temperatures may be useful to demonstrate the temperature acceleration.

Following the work of Berman [5], the time to failure under a TDDB condition (t_{BD}) for any component of the failed fraction (t_{63}, t_1, …) can be obtained from the failure distribution obtained from a V-Ramp test:

$$t_{BD} = t_0*\exp[\gamma(E_R-E_{use})] \quad \text{(B.6)}$$

where t_0 is an effective time constant, γ is the field acceleration parameter in [cm/V], E_R is the measured (ramped) breakdown field, and E_{use} is the use field for which t_{BD} is to be determined. If E_R for the t_{63} fail is used, then the t_{BD} obtained is the t_{63} failure percentile at the E_{use} value.

The time constant t_0 can be written as: $t_0 = \Delta t/[1-\exp(-\gamma*\Delta E)]$, or it can be simplified as $t_0 = 1/(\gamma*R)$, where R is the constant ramp rate $\Delta E/\Delta t$.

The field acceleration parameter γ can be obtained if populations are taken to failure using different ramp rates; determined by the slope of $\ln(t_{BD})$ plotted versus the failure field.

Annex C (Informative) Bibliography

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